REMARKS

Remaining Claims

Claims 1, 2, 4, and 6 – 20 remain pending in this application. Claim 3 has been cancelled. Claims 1, 2, 4, 11, 14, 15, 19 and 20 have been amended herein. New claims 21 – 24 have been added. As explained in more detail below, the Applicant respectfully submits that all claims are in condition for allowance and respectfully request such action.

Rejection of Claims 2-5 and 11-18 under 35 USC §112, second paragraph

Claims 4 and 16 stand rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Applicant respectfully traverses the rejection and requests reconsideration.

The Examiner refers to language in claims 2, 5 and 11 that the Examiner believes renders these claims indefinite. With respect to claim 2, the Applicant has amended that claim to ensure that there are no problems with indefiniteness or antecedent basis. With respect to the Examiner's objection to the use of the phrase "said first one of said first flip flops" in lines 7 – 8 of claim 2, this language has been changed to "said first one of said flip flops". With respect to the phrase "said first clock" in lines 10 – 11 of claim 2, the Applicant respectfully submits that this is correct. The synchronization logic of the embodiment shown in Fig. 1 may include one or more flip flops, such as flip flops 6 and 7 shown in Fig. 2, although claim 2 is not limited to such a construction. Both of these flip flops are clocked by the first clock, which is clock A in Fig. 2.

With respect to the phrase "to enable data from the first and second data paths to be selectively combined", this language has been replaced with other language, which the Applicant believes is better describes this feature of the invention. With respect to the Examiner's comment that "Data Out output logic" in lines 15 – 21 of claim 2 is misdescriptive, the Applicant respectfully submits that it is not because Fig. 1 shows an output flip flop 9, which corresponds to the output flip flop of the Data Out output logic recited in claim 2.

With respect to claim 5, the Examiner states that the phrase "said first one of said first flip flops does not have a clear antecedent basis. This phrase has been changed to "said first one of said flip flops".

With respect to claim 11, the Examiner states that the phrase "the synchronization flip flop" in lines 15 – 16 lacks antecedent basis. This phrase has been changed to "said at least one synchronization flip flops". The Examiner states that "the first clock" in line 16 is incorrect. This phrase has been changed to "the second clock". The Applicant apologizes for the oversight. The Examiner states that the description of "output logic" in lines 21 – 25 appears to be misdescriptive because there is no output flip flop in Fig. 3. The Applicant respectfully submits that the description is correct because the output logic in Fig. 3 includes output flip flop 36 and/or output flip flop 37, although claim 11 is not limited to this construction.

For all of these reasons, the Applicant respectfully submits that this rejection is overcome and requests that it be withdrawn.

Rejection of Claims 1, 6-10 and 19-20 under 35 USC §102(b) – Gujral et al.

Claims 1, 6-10 and 19-20 are rejected under 35 USC §102(b) as being anticipated by Gujral et al. (U.S. Patent No. 5,896,052). Generally, the Examiner indicates that Gujral et al. discloses all of the elements recited in claims 1, 6 – 10, 19 and 20. This rejection is believed to be moot in view of the amendments to independent claims 1, 19 and 20.

The Examiner has not rejected any of claims 2 – 5 or 11 – 18 based on prior art. Independent claims 1, 19 and 20 have been amended to incorporate the subject matter of claim 3, which is believed to be allowable over the prior art of record. Specifically, these claims have been amended to recite "wherein logic gates of the first clock domain logic that are in a signal path that is coupled to the input of the first input flip flop are provided by the synchronizer with a first clock cycle as a setup time margin."

One of the primary features of the synchronizer of the present invention is that it greatly increases the setup time margin for the logic upstream of the synchronizer because the data input to the synchronizer does not have to be valid until the very end of the first clock cycle. Independent claims 1, 19 and 20 have been amended to recite this feature of the present invention, which is neither taught nor suggested by the prior art of record. Accordingly, the Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

New Claims 21 – 24

Claims 21 and 23 have been added to cover the feature of the present invention that the synchronizer is synchronizes data of a first clock domain to a second clock domain where the ratio of the first clock to the second clock is a non-integer. Claims 22 and 24 have been added to cover the feature of the present invention that the synchronizer is synchronizes data of a first clock domain to a second clock domain where the ratio of the second clock to the first clock is a non-integer. The Applicant does not believe that the prior art of record teaches or suggests this feature of the present invention, support for which can be found on, for example, page 4, lines 1 - 7 and page 7 lines 14 – 16 of the specification.

CONCLUSION

For the reasons set forth above, it is respectfully submitted that all pending claims are now in condition for allowance, and Applicant requests a Notice of Allowance be issued in this case. Should there be any further questions or concerns, the Examiner is urged to telephone the undersigned to expedite prosecution.

Respectfully submitted,
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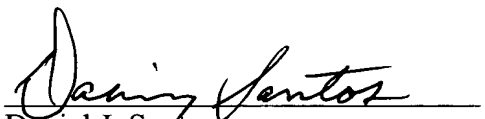

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